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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/371,955	08/11/1999	SHANE P. LEIPHART	M4065.0196/P	9847

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EXAMINER	
KANG, DONGHEE	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/371,955	LEIPHART, SHANE P.	
	Examiner	Art Unit	
	Donghee Kang	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **26-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al. (US 5,312,775) in view of Cerio, Jr. (US 6,268,284).

Fujii et al. teach a semiconductor device, comprising (Fig.5J):

a metallic layer (4) over a substrate (1); a dielectric layer (5) over said metallic layer; a via hole extending through the dielectric layer to a surface of the metallic layer; a titanium aluminide layer lining at least a bottom of the via hole; and a conductive material (103) on the titanium aluminide layer being in contact at an interface.

Fujii et al. do not teach a titanium aluminide layer on sides of said via hole. However, Cerio, Jr. teaches a depositing a titanium aluminide ($TiAl_3$) on the bottom and sidewalls of via 40 using sputtering method. In Cerio's device, omission of the annealing step results in a reducing stress voiding since there is no reaction in the via. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use sputtering method for depositing the titanium aluminide layer lining a bottom and sides of the via since the sputtering method reduces the stress voiding in the via hole.

Fujii et al. as modified by Cerio do not expressly teach the interface is substantially free from tensile stress between said titanium aluminide layer lining a bottom of the via hole and said conductive material. However, this feature is inherent because the conductive layer (72) is deposited after forming titanium aluminide layer.

3. Claims **28-35 & 37-40** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al. (US 5,312,775) in view of Cerio, Jr. (6,268,284) and further in view of Fiordalice et al. (US 5,358,901)

Re claims **28-32**, the teaching of Fujii et al. as modified by Cerio, Jr. was discussed above in section 2. See a statement of rejection of claims 26-27.

Fujii et al. teach a memory circuit region in a semiconductor substrate. Fujii et al. do not teach the semiconductor device further comprising an antireflective coating over said first metallic layer. However, it is common to use a layerer of material to suppress reflections from underlying surface during photolithography exposure steps and also Fiordalice et al. teach in Fig.8 forming the antireflective coating (42) over the first metallic layer. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to for antireflective coating layer in Fujii's as modified by Cerio as taught by Fiordalice since antireflective coating layer suppresses reflections underlying layers so that the photoresist is not exposed to the reflected light wave which leads to variation in critical dimension.

Re claims **33-35 & 37-40**, prior arts do not expressly teach a substrate comprising a memory module. However, it would have been obvious to one of ordinary

skill in the art at the time the invention was made to have module system, since module system includes a plurality of components each storing or reading on binary bit at a time in the semiconductor memory device.

4. Claims **36** is rejected under 35 U.S.C. 103(a) as being unpatentable over Clayton (US 4,656,605) in view of Harada et al. (US 5,313,101).

Clayton teaches a memory module, comprising (Fig.2 & Col.2, lines 49-57):

a substrate comprising a circuit board (Col.2, lines 50-52); a plurality of memory chips (10-18) mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprising a random access memory (RAM) fabricated on a semiconductor substrate; and a connector on the substrate, said connector being wired to said memory circuit. Clayton does not expressly teach that the memory chip comprises a random access memory fabricated on a semiconductor substrate comprising:

a memory circuit region in the semiconductor substrate; a first dielectric over the memory circuit region; a first metallic layer, said first metallic layer comprising aluminum; a contact interconnect between the first metallic layer and the substrate; a second dielectric layer over the first metallic layer; a via hole extending through the second dielectric layer to a surface of the first metallic layer; a titanium aluminide layer lining a bottom of the via hole; a conductive plug material on the titanium aluminide layer, said conductive plug material comprising aluminum; and a second metallic layer on the second dielectric layer and electrically connected to the conductive plug material.

Harada et al. teach a semiconductor integrated circuit device, comprising (Fig.1 & Col.8, line 50 – Col.9, line 11):

a memory circuit region (2) in a semiconductor substrate; a first dielectric (3) over the memory circuit region; a first metallic layer (4), said first metallic layer comprising aluminum (Col.8, lines 58); a contact interconnect between the first metallic layer and the semiconductor substrate; a second dielectric layer (5) over the first metallic layer; a via hole extending through the second dielectric layer to a surface of the first metallic layer; a titanium aluminide layer (206) lining a bottom of the via hole; a conductive plug material (103) on the titanium aluminide layer, said conductive plug material comprising aluminum; and a second metallic layer on the second dielectric layer and electrically connected to the conductive plug material. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the semiconductor integrated device as taught by Harada into the memory module of Clayton since the titanium aluminide intermetallic layer helps to reduce the electron-migration and stress-migration at the via hole.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 571-272-1656. The examiner can normally be reached on Maxiflex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Donghee Kang
Examiner
Art Unit 2811

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